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DICKEY, THOMAS L	
ART UNIT	**PAPER NUMBER**
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,793	BHATTACHARYYA, ARUP	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-79* is/are pending in the application.

4a) Of the above claim(s) *See Continuation Sheet* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-4,6,7,20,21,25,26,32-34,37,39,63-65,67,69,71-74 and 77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-79* are subject to restriction and/or election requirement.

/Thomas L. Dickey/
Primary Examiner
Art Unit 2826

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/09/2008 and 11/10/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims withdrawn from consideration are 5,8-19,22-24,27-31,35,36,38,40-62,66,68,70,75,76,78 and 79.

DETAILED ACTION

Election/Restriction

1. Applicant's election with traverse of the species of Embodiment 1 (as described in words and figures in shown in figures 6A-6B and paragraphs 0069-0072) in the reply filed on 12/27/07 is acknowledged.

Applicant has stated that claims 1-7, 13, 17-21, 25-26, 32-34, 37, 39, 42-44, 48-49, 51, 56- 58, 60, 62, 63-69, 71-74, 76-77 read on[1] the elected embodiment. Claims 8-12, 14-16, 22-24, 27-31, 35, 36, 38, 40-41, 45-47, 50, 52-55, 59, 61, 70, 75, 78-79 are therefore withdrawn. Claims 56-58, 60, and 62, which depend from withdrawn claim 54, are also withdrawn.

Furthermore, only claims that "read on" (using Applicants" phrase) the elected embodiment may be considered after election. Claims 5, 13, 17, 18, 19, 42-53, 57, 66, and 76 require a semiconductor-on-insulator structure. The elected embodiment does not include a semiconductor-on-insulator structure. Claims 5, 13, 17, 18, 19, 42-53, 57, 66, and 76 do not read on the elected embodiment because the elected embodiment

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[1] Note that "A claim reads on something, if every element of that claim is present in that which it reads on." See http://www.delphion.com/help/glossary#readon. "Read on" has the same meaning regardless of whether it is used to determine infringement, anticipation, obviousness, new matter issues, or

does not include a semiconductor-on-insulator structure. Because claims 5, 13, 17, 18, 19, 42-53, 57, 66, and 76 do not read on the elected embodiment, claims 5, 13, 17, 18, 19, 42-53, 57, 66, and 76 are withdrawn from consideration. Claim 68 requires a vertically-oriented diode. The elected embodiment does not include a vertically oriented diode. Claim 68 does not read on the elected embodiment because the elected embodiment does not include a vertically-oriented diode. Because claim 68 does not read on the elected embodiment, claim 68 is withdrawn from consideration.

2. Applicant's traversal is on the ground(s) "that the restriction is improperly conclusory." Applicant continues, "In particular, the Office states: 'The species are independent or distinct because claims to the different species recite the mutually exclusive characteristics of such species. In addition, these species are not obvious variants of each other based on the current record.' Accordingly, the Office Action fails to identify the 'mutually exclusive characteristics of such species' that serve as the basis of the restriction as required in MPEP 803." This is not found persuasive because there is no requirement in either § 803 or § 804.04(f) (which deals with restrictions between species) that an Office Action identify the mutually exclusive species. § 804.04(f) merely

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restrictability, The phrase "read on" is often used by patent professionals. The examiner cites Delphion's definition because it appears representative of the common understanding of patent professionals.

requires 1) that the various species actually be mutually exclusive; and 2) that various claims be directed to the various species.

In the present case, the mutually exclusive features of the species are self-evident. Some species require bulk substrates (as the elected species does), while some species require SOI substrates. A substrate cannot simultaneously be bulk and SOI. Some species require vertically oriented diodes (as the elected species does); others require laterally oriented diodes. Does Applicant argue that a diode can simultaneously be vertically and laterally oriented? Other mutually exclusive features (such as the distinction between figure 23's laterally oriented un-gated diode, embedded in the substrate, and the laterally oriented gated diode formed over the substrate seen in figure 22) of the species are equally apparent.

Applicant's traverse appears to be based on the restirction's failing an alleged "pro forma" requirement. This alleged "pro forma" requirement is not actually found in the MPEP. Therefore, the requirement is still deemed proper and made FINAL.

Information Disclosure Statement

3. The Information Disclosure Statements filed on 07/09/2008 and 11/10/2008 have been considered.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74, and 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over NEMATI ET AL. (6,229,161) in view of KRIVOKAPIC (6,291,832). In the examiner's opinion, this/these claim(s) would have been obvious according to one of the rationales expressed in the *Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in View of the Supreme Court Decision in KSR International Co. v. Teleflex Inc.*, as published at 72 Federal Register 57526 et seq.[2] (10/10/2007).

The Guidelines explain that an invention that would have been obvious to a person of ordinary skill at the time of the invention is not patentable. The Guidelines point out that, as reiterated by the Supreme Court in KSR, the framework for the objective analysis for determining obviousness under 35 U.S.C. 103 is stated in *Graham v. John*

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[2] Available at http://www.uspto.gov/web/offices/com/sol/notices/72fr57526.pdf See also MPEP, Eighth Ed. Rev. 6 (Sept. 2007) §§ 2141 et seq., available at http://www.uspto.gov/web/offices/pac/mpep/documents/2100.htm Please note that §§ 2141 et seq. have been completely revised, in view of KSR v. Teleflex.

Deere Co. Obviousness is a question of law based on underlying factual inquiries. The factual inquiries enunciated by the Court are as follows:

(1) Determining the scope and content of the prior art;

(2) Ascertaining the differences between the claimed invention and the prior art, and

(3) Resolving the level of ordinary skill in the pertinent art.

Examining this last factor first, it is noted that any obviousness rejection should include, either explicitly or implicitly in view of the prior art applied, an indication of the level of ordinary skill. This is an essential finding because (as the Guidelines point out) a finding as to the level of ordinary skill may be used as a partial basis for a resolution of the issue of obviousness. The person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. Factors that may be considered in determining the level of ordinary skill in the art include:

(1) "Type of problems encountered in the art;"

(2) "prior art solutions to those problems;"

(3) "rapidity with which innovations are made;"

(4) "sophistication of the technology;" and

(5) "educational level of active workers in the field".

In a given case, every factor may not be present, and one or more factors may predominate.

In the present case, Applicant has presented claims to a device classified in Class

257 (Semiconductor Devices). The types of problems encountered in Class 257 typically are highly complex, involving questions of electrodynamics, thermodynamics, crystallography, and quantum mechanics. Prior art solutions to the problems presented in this field demonstrate thinking of the highest order. Many prior art solutions in this field have won Nobel prizes. Past Nobel prizewinners for Class 257 innovations include John Bardeen, William Schockley, Jack Kilby, Leo Esaki, Nick Basow, Zhores Alferov, Pierre-Gilles de Gennes, and probably a half dozen more this writer has forgotten. Note, for example, that the most recent Nobel Prize in physics went to Albert Fert and Peter Grünberg for an innovative solution to the problem of Giant Magnetic Resonance, a solution now incorporated into many semiconductor memory devices. Innovations in Class 257 are made with extremely high rapidity (see, e.g. "Moore's Law"). Technology used to make and practice inventions in this field are highly sophisticated. Some "fabs" (as those of skill in the art call the factories for making these devices) now cost in excess of one billion dollars each, and perform literally hundreds of billions of operations per hour. Finally, the educational level of active workers in this field is extremely high – Ph.D.s are common, and a bachelor's degree in engineering is the absolute minimum educational level of workers in this field.

In short, the level of ordinary skill in this field is extremely high. In *KSR* (while considering an invention involving the substitution of one simple mechanical linkage for

another), the Supreme Court cautioned, "A person of ordinary skill is also a person of ordinary creativity". *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1742, 82 USPQ2d 1385, 1397 (2007). Had the Court been looking at the variety of extraordinarily valuable (from lifestyle-changing, such as high-speed communications and computing, to handy devices such as IPods and cellphones) and difficult solutions to challenging problems that have been accomplished in the semiconductor art in recent years, the Court might easily have said that in the semiconductor art the person of ordinary skill is a person of extraordinary creativity.

Next, we consider the first and second factual findings required by *Graham*. With regard to claims 1-4 the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell comprising an access transistor 12 formed in a bulk semiconductor structure (substrate P-sub) and having a floating node (second diffusion region 24) and a device exhibiting Negative Differential Resistance (NDR) behavior connected between the floating node (second diffusion region 24) and a reference potential line 19, the device including an anode and a cathode connected to the floating node (second diffusion region 24) of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al.

With regard to claim 6 the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell comprising an access transistor 12 having a first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18, and a second diffusion region 24 a Negative Differential Resistance (NDR) device connected between the second diffusion region 24 and a reference potential line 19, the device including an anode and a cathode. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al.

With regard to claim 7 the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell comprising an n-channel access transistor 12 on a bulk semiconductor substrate P-sub, the n-channel access transistor 12 having a first n-type diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a second n-type diffusion region 24 and a Negative Differential Resistance (NDR) device having an n-type anode connected to a device reference potential line 19 and a p-type cathode in contact with the second n-type diffusion region 24. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al.

With regard to claims 20,21,25,26, and 32, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell comprising an access transistor 12 including an n-channel transistor on a bulk semiconductor

substrate P-sub, including a body region (bulk substrate P-sub) a first diffusion region (not numbered; seen directly under bit line 18) electrically connected to a bit line 18 a second diffusion region 24 separated from the first diffusion region by a channel area in the body region (bulk substrate P-sub) a gate 14 separated from the channel area by a gate insulator (not numbered; seen under gate 14), the gate 14 electrically connected to a word line a Negative Differential Resistance (NDR) device, including an anode and a cathode, the device being connected between the second diffusion region 24 and a reference potential line 19, wherein the device has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the device and the memory cell is operative to store and sense a charge in the second diffusion region 24 that is representative of a memory state. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al.

With regard to claims 33,34,37, and 39, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell comprising an access transistor 12 formed in a bulk semiconductor structure, the access transistor 12 including a first diffusion region (not numbered; seen directly under bit line 18) separated from a second diffusion region 24 by a channel region, and further including a gate 14 separated from the channel region by a gate insulator (not numbered; seen under gate 14), wherein the first diffusion region is connected to a bit line 18 and the

gate 14 is connected to a first word line and a vertically-oriented gate-controlled Negative Differential Resistance (NDR) device connected between a reference potential line 19 and the second diffusion region 24, the device including an anode and a cathode, and an operably positioned gate 20, the gate 20 being connected to a second word line WL1. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al.

With regard to claims 63-65, 67, 69, and 71, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell comprising an access transistor 12 including an n-channel transistor, a first diffusion region (not numbered; seen directly under bit line 18) separated from a second diffusion region 24 by a channel region, and a gate 14 separated from the channel region by a gate insulator (not numbered; seen under gate 14), wherein the first diffusion region is connected to a bit line 18 and the gate 14 is connected to a first word line; and a vertically-oriented Negative Differential Resistance (NDR) device connected between a reference potential line 19 and the second diffusion region 24, the NDR device including an n-type anode and a p-type cathode, wherein the device has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the device and wherein the access transistor 12 and the device are on a bulk

semiconductor substrate P-sub. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al.

With regard to claims 72-74 and 77 the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell comprising a memory array, including a plurality of memory cells in rows and columns a number of word lines, each word line connected to a row of memory cells a number of bit lines, each bit line 18 connected to a column of memory cells at least one reference line to provide a reference potential to the memory cells control circuitry, including word line select circuitry and bit line select circuitry to select a number of memory cells for writing and reading operations, wherein each memory cell includes an access transistor 12, including a body region (bulk substrate P-sub), a first diffusion region (not numbered; seen directly under bit line 18) electrically connected to one of the bit lines, a second diffusion region 24 separated from the first diffusion region by a channel area in the body region (bulk substrate P-sub), and a gate 14 separated from the channel area by a gate insulator (not numbered; seen under gate 14) and electrically connected to one of the word lines and a vertically-oriented Negative Differential Resistance (NDR) device, including an anode and a cathode, the device being connected between the second diffusion region 24 and a reference line (reference potential line 19), wherein the device has a structure to allow the memory cell to switch memory states using a forward or

reverse bias voltage across the device, wherein the memory cell is adapted to store a charge in the second diffusion region 24 of the access transistor 12 to indicate a stable memory state and wherein the device includes a gate-controlled device and the memory device is adapted to gate the gate-controlled device to enhance switching between memory states, wherein the vertical-oriented device is at least partially formed in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al.

The applicant's claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74, and 77 do not distinguish over the Nemati et al. reference regardless of the claims reciting the performing of certain function(s) using the claimed device, because only the device per se is relevant, not the recited functions of using the floating node for storing a charge indicative of a memory state of the memory cell.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to

perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); *Ex parte* Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"); *Ex parte* THOMAS J. WHALEN II, slip opinion[3], page 13, (BPAI, PRECEDENTIAL, decided July 23, 2008) ("'[T]he examiner must provide some evidence or scientific reasoning to establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art' before the burden is shifted to the applicant to disprove the inherency"); and *Leggett & Platt Inc. v. VUTEk Inc.*, 537 F3d 1349, 1352, 87 USPQ2d 1947, 1951 (Fed. Cir. 2008) ("Moreover, because the claim is written with functional rather than structural language—it requires the cold UV assembly to be 'effective to' substantially cure rather than requiring ink to be substantially cured—the claim limitation will be anticipated so long as the LEDs disclosed in the '823 patent are able to cure the ink to a great extent"). See MPEP § 2114.

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[3] Available at the BPAI website as http://www.uspto.gov/web/offices/dcom/bpai/prec/fd074423.pdf

In this case, it is reasonable to predict that Nemati et al.'s device is capable of using the floating node for storing a charge indicative of a memory state of the memory cell, because a comparison of Applicant's specification to Nemati et al.'s disclosure reveals that Nemati et al. discloses a device that is apparently identical to the device Applicant describes as being capable of performing the function(s) of using the floating node for storing a charge indicative of a memory state of the memory cell.

Because it is reasonable to predict that assume that Nemati et al.'s device is capable of performing the claimed function, the burden shifts to Applicants to come forward with evidence showing that the prior art device, despite reasonable appearances, is not so capable. See MPEP § 2114.

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim requires a negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode, Nemati et al.'s memory cell includes a negative differential resistance NPNP thyristor device.

However, Krivokapic discloses a negative differential resistance diode including an n/i/p diode having an n+ anode 204, a p cathode 206, and an intrinsic region 208 between the anode 204 and cathode 206. Note figure 5, column 3 lines 61-67, and column 4 lines 1-6 of Krivokapic.

The n/i/p diode of applicant's claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74, and 77 does not distinguish over that of the Krivokapic reference regardless of the claims' reciting the performing of certain function(s) using the claimed diode, because only the device per se is relevant, not the recited functions of using the geometry of intrinsic region of the diode for assisting with stabilizing the memory state of the memory cell and allowing the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); *Ex parte* Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are

produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"); *Ex parte* THOMAS J. WHALEN II, slip opinion, page 13, (BPAI, PRECEDENTIAL, decided July 23, 2008) ("'[T]he examiner must provide some evidence or scientific reasoning to establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art' before the burden is shifted to the applicant to disprove the inherency"); and *Leggett & Platt Inc. v. VUTEk Inc.*, 537 F3d 1349, 1352, 87 USPQ2d 1947, 1951 (Fed. Cir. 2008) ("Moreover, because the claim is written with functional rather than structural language—it requires the cold UV assembly to be 'effective to' substantially cure rather than requiring ink to be substantially cured—the claim limitation will be anticipated so long as the LEDs disclosed in the '823 patent are able to cure the ink to a great extent"). See MPEP § 2114.

In this case, it is reasonable to predict that Krivokapic's n/i/p diode is capable of using the geometry of intrinsic region of the diode for assisting with stabilizing the memory state of the memory cell and allowing the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode, because a comparison of Applicant's specification to Krivokapic's disclosure reveals that Krivokapic discloses a diode that is apparently identical to the diode Applicant

describes as being capable of performing the function(s) of using the geometry of intrinsic region of the diode for assisting with stabilizing the memory state of the memory cell and allowing the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode.

Because it is reasonable to predict that assume that Krivokapic's diode is capable of performing the claimed function, the burden shifts to Applicants to come forward with evidence showing that the prior art device, despite reasonable appearances, is not so capable. See MPEP § 2114.

The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74, and 77 by substituting the negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode taught by Krivokapic for Nemati et al.'s negative differential resistance NPNP thyristor device.

To reject a claim on the basis of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

> (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
>
> (2) a finding that the substituted components and their functions were known in the art;

(3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and

(4) whatever additional findings based on the *Graham* factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode) for other components (a negative differential resistance NPNP thyristor device). Krivokapic discloses that the substituted components and their functions were known in the art. Further, Krivokapic discloses that those of skill in the art were familiar with a negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode where tunneling occurs through a potential barrier having a very narrow width, so that the frequency response of a resonant tunneling device is not limited by the diffusion or transit time of charge carriers. Instead, the frequency response is limited only by the circuit capacitance and impedance of the device, generating an improved response over the negative differential resistance NPNP thyristor device used in Nemati et al.'s memory cell. From the similarities between the negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode and Nemati et al.'s negative differential resistance NPNP thyristor device, one of skill in the art would have been able to conclude that negative differential n/i/p diode having an n+ anode, a p

cathode, and an intrinsic region between the anode and cathode could have substituted for the negative differential resistance NPNP thyristor device of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on its functioning in Krivokapic's disclosure) that negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode would have continued functioning in Nemati et al.'s memory cell much as it did in Krivokapic's disclosure, and that after the substitution, Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode taught by Krivokapic for Nemati et al.'s negative differential resistance NPNP thyristor device.

B. The Guidelines point out that the both the Graham and KSR decisions require Office personnel to evaluate objective evidence relevant to the issue of obviousness. Such evidence, sometimes referred to as "secondary considerations," may include evidence of commercial success, long-felt but unsolved needs, failure of others, and unexpected results. The evidence may be included in the specification as filed, accompany the application on filing, or be provided in a timely manner at some other point during the prosecution. The weight to be given any objective evidence is decided

on a case-by-case basis. The mere fact that an applicant has presented evidence does not mean that the evidence is dispositive of the issue of obviousness.

For evidence of unexpected results, one must rely solely on evidence supplied by Applicants. Applicants have actually made the claimed combination. Evidence of differences between results of the actual functioning of the claimed combination and the results of the functioning one of skill in the art would have had reason to predict (i.e., the "expected results") must necessarily come from one who has actually made the combination. A clear case of unexpected results would be if the claimed combination of prior art elements did not in fact perform according to their established functions in a predictable fashion; a result sometimes referred to as "synergy". See *Anderson's-Black Rock v. Pavement Co.* 396 U.S. 57, 61 (1969) (note that the *Anderson's-Black Rock* opinion does not actually employ the word "synergy"). However, the Guidelines make it clear that any type of unexpected results (and indeed any type of secondary considerations) must be considered.

Applicants' specification, however, does not include any evidence of secondary considerations. Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

Response to Arguments

5. Applicant's arguments with respect to claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74, and 77 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thomas L. Dickey/
Primary Examiner
Art Unit 2826